CLAIMS

We claim:

5   **1.** A flip-flop circuit comprising:

        (a) a first branch having two transistors in series and a source node;

        (b) a second branch having two transistors in series and a source node, said source node being common with said source node of said first branch;

        (c) a shared transistor having its source connected to said source nodes of said

10   first and second branches; and

        (d) a pulse generator connected to the gate of said shared transistor.

    2. The flip-flop circuit of claim **1** wherein:

        (a)   said first branch comprises a P type transistor and an N type transistor

15   connected in series, the source of said N type transistor being connected to said source node and the drain of said P type transistor being connected to a high potential; and

        (b)   said second branch comprises a P type transistor and an N type transistor connected in series, the source of said N type transistor being connected to said

20   source node and the drain of said P type transistor being connected to a high potential.

3. The flip-flop circuit of claim 2 wherein the source of said first branch P-type transistor is connected to a first branch latch and the source of said second branch P-type transistor is connected to a second branch latch.

4. The flip-flop circuit of claim 3 wherein said latches include means for retaining the value in said latch even when disconnected from the circuit.

5. The flip-flop circuit of claim 4 wherein said value retaining means includes back to back inverters, one inverter being selected to be weaker than the other inverter.

6. The flip-flop circuit of claim 2 wherein said shared transistor is an N type transistor.

7. The flip-flop circuit of claim 1 wherein said pulse generator comprises:

    (a)   an inverter chain having:

        (i) an input node for received a clock signal; and

        (ii) an output;

    (b)   a NAND having an output and two inputs, one said NAND input connected to said inverter chain input node and one said NAND input connected to said output of said inverter chain; and

    (c)   an inverter having an input and an output, said inverter input connected to said output of said NAND and said inverter output connected to the gate of said shared transistor.

8. The flip-flop circuit of claim 2 further comprising:

(a)   a data signal input connected to the gates of said first branch P type transistor and said first branch N type transistor; and

5   (b)   a data inverter having an input and an output, said data signal inverter input connected to said data signal input and said data inverter output connected to the gate of said second branch N type transistor.

9. The flip-flop circuit of claim 3 further comprising:

10   (a)   a data signal input connected to the gates of said first branch P type transistor and said first branch N type transistor; and

(b)   a data inverter having an input and an output, said data signal inverter input connected to said data signal input and said data inverter output connected to the gate of said second branch N type transistor.

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10. A flip-flop circuit comprising:

(a)   a first branch comprising a P type transistor and an N type transistor connected in series, the drain of said P type transistor being connected to a first branch

20   drain node and the source of said N type transistor being connected to a low potential;

(b)   a second branch comprising a P type transistor and an N type transistor connected in series, the drain of said P type transistor being connected to a second

branch drain node and the source of said N type transistor being connected to a low potential, said drain node being common with said drain node of said first branch

(c) a shared transistor having its drain connected to said drain nodes of said first and second branches; and

5   (d) a pulse generator connected to the gate of said shared transistor.

11. A static explicit pulsed flip-flop circuit comprising:

(a) a first branch having three transistors in series, one of said first branch transistors being a clocked transistor and the other two transistors being non-clocked

10   transistors having their gates connected to a data input;

(b) a second branch having three transistors in series, one of said second branch transistors being a clocked transistor and the other two transistors being non-clocked transistors having their gates connected to a node between said first branch non-clocked transistors; and

15   (c) a pulse generator connected to the gates of said clocked transistors in said first and second branches.

12. The flip-flop circuit of claim 11 wherein said gates of said second branch non-clocked transistors are connected to a first branch latch and a second branch latch is

20   connected between said second branch non-clocked transistors.

13. The flip-flop circuit of claim 12 wherein said latches include means for retaining the value in said latch even when disconnected from the circuit.

14. The flip-flop circuit of claim 13 wherein said value retaining means includes back to back inverters, one inverter being selected to be weaker than the other inverter.

15. The flip-flop circuit of claim **11** wherein:

   (a)   said first branch clocked transistor and said second branch clocked transistors are N type transistors;

   (b)   one of said non-clocked first branch transistors is a P type transistor, one of said non-clocked first branch transistors is an N type transistor, and said first branch N-type transistor is connected to said first branch clocked transistor; and

   (c)   one of said non-clocked second branch transistors is a P type transistor, one of said non-clocked second branch transistors is an N type transistor, and said second branch N-type transistor is connected to said second branch clocked transistor.